

Fig. 1

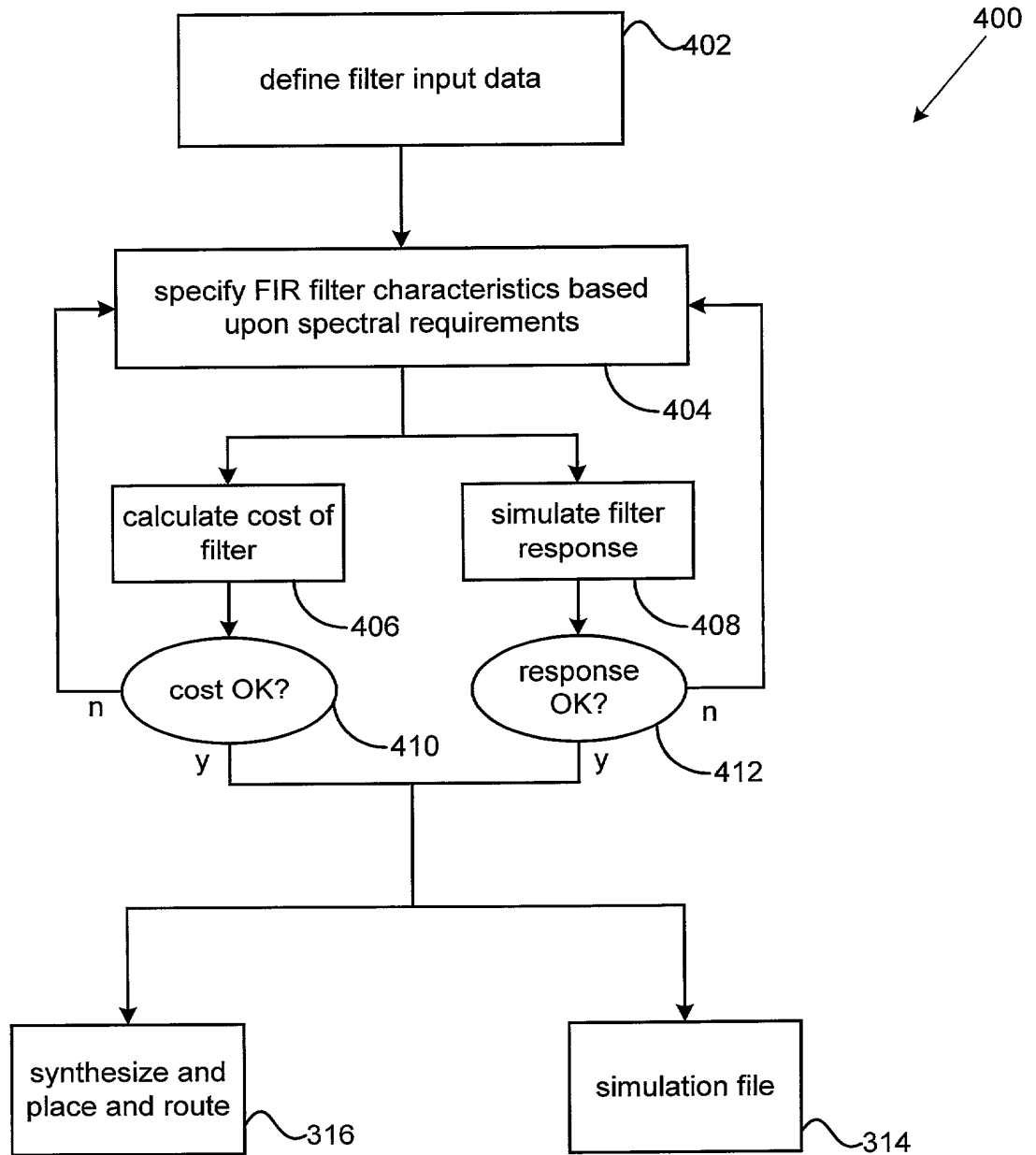


Fig. 2

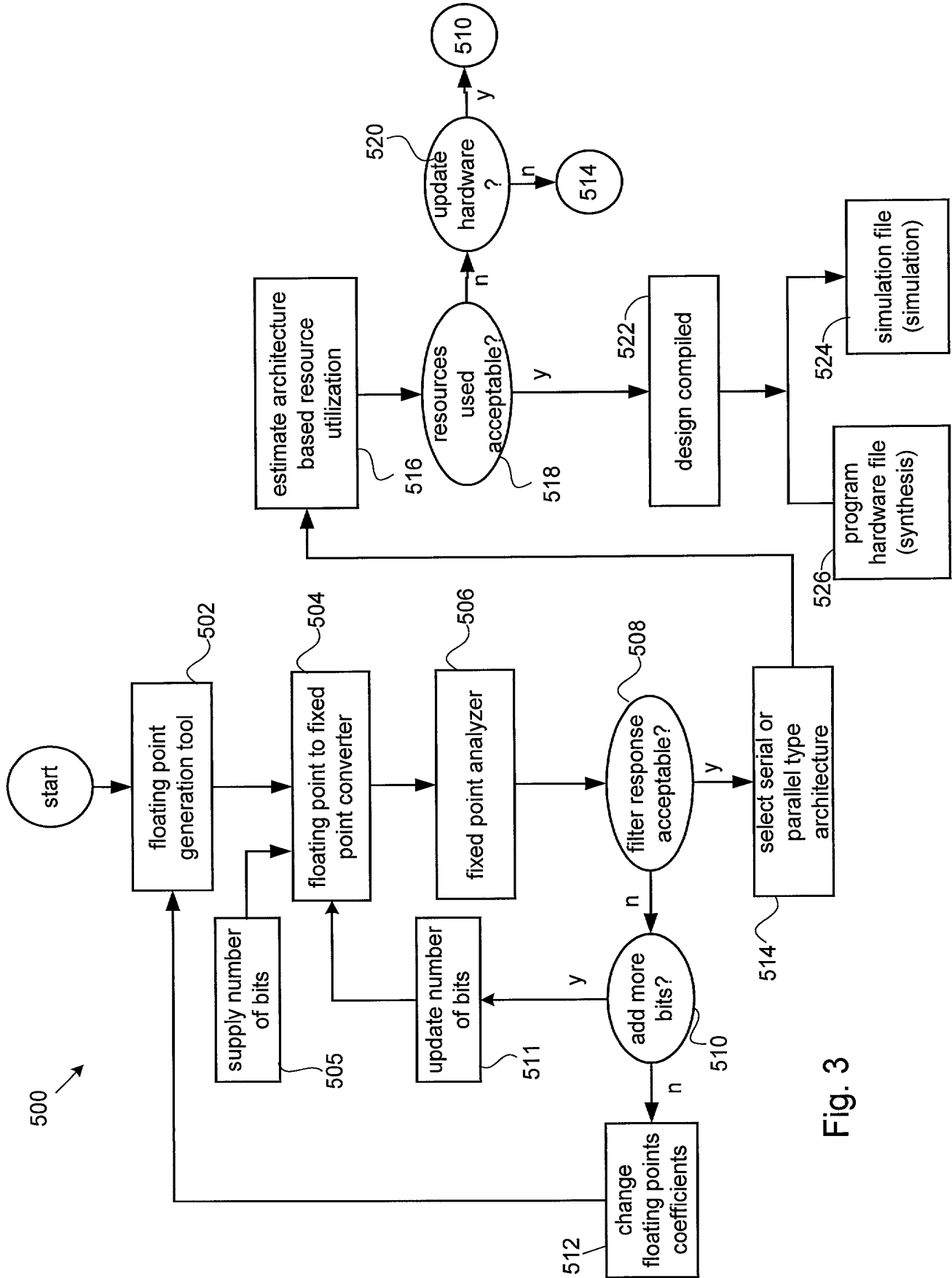


Fig. 3

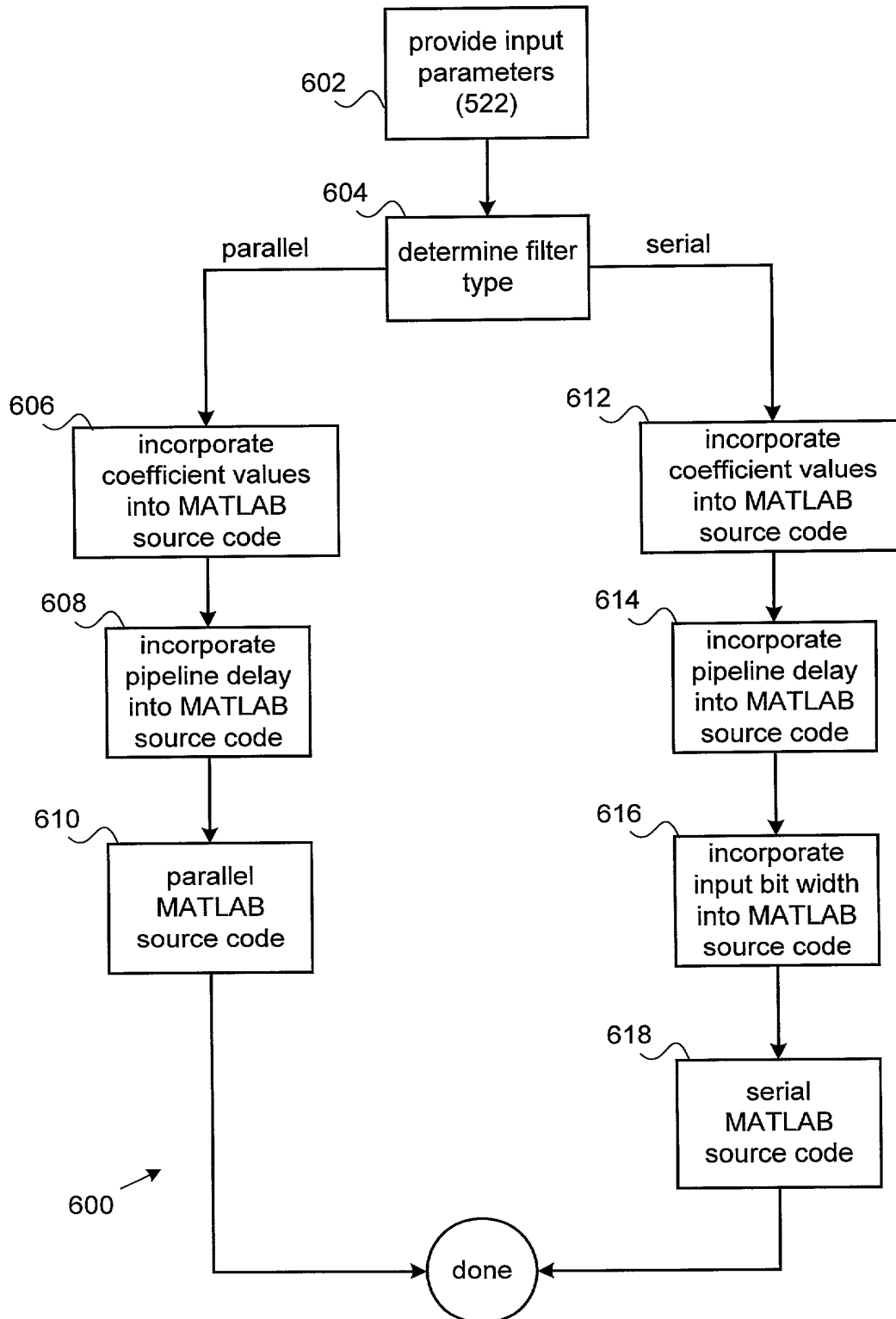
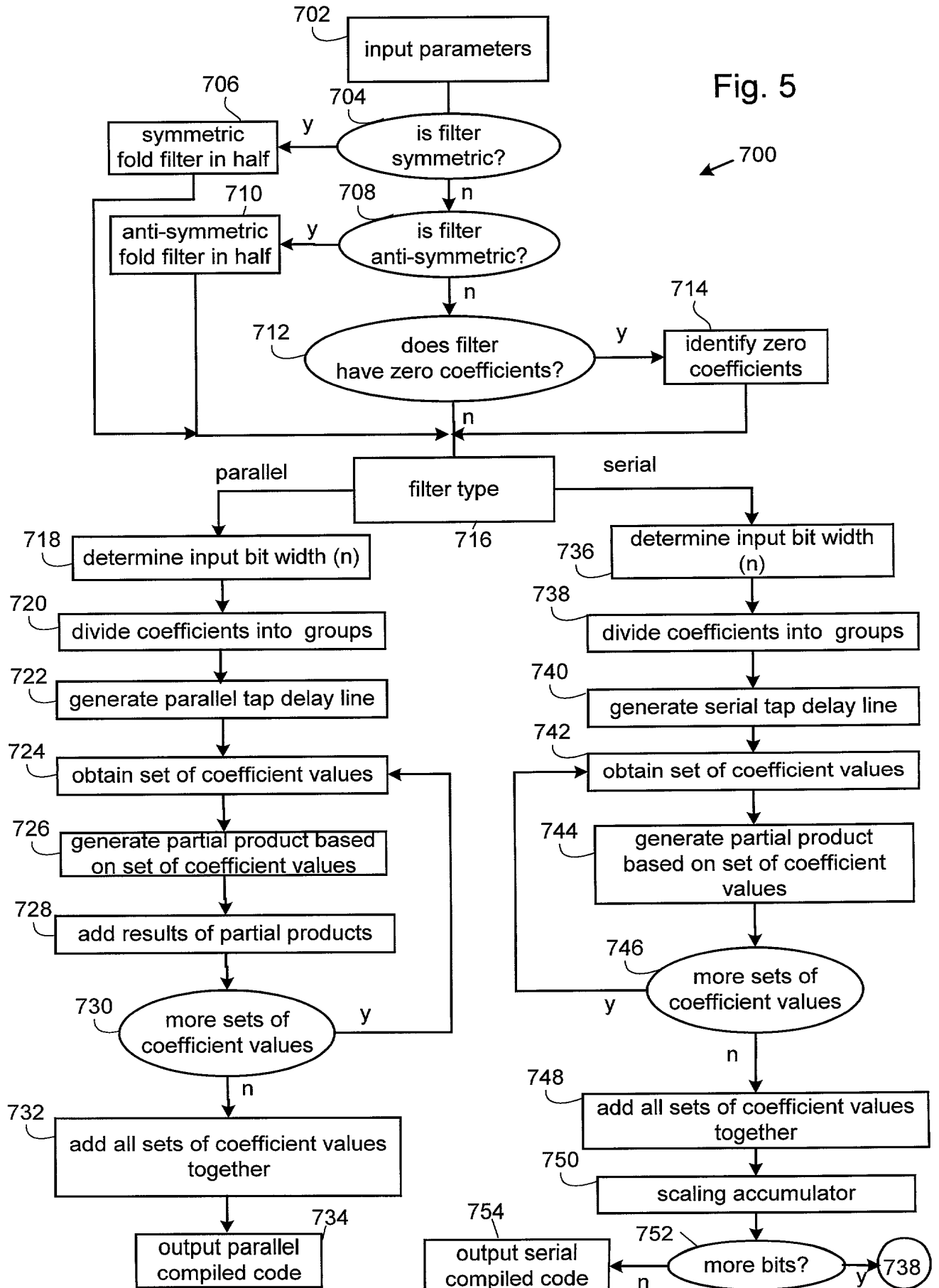
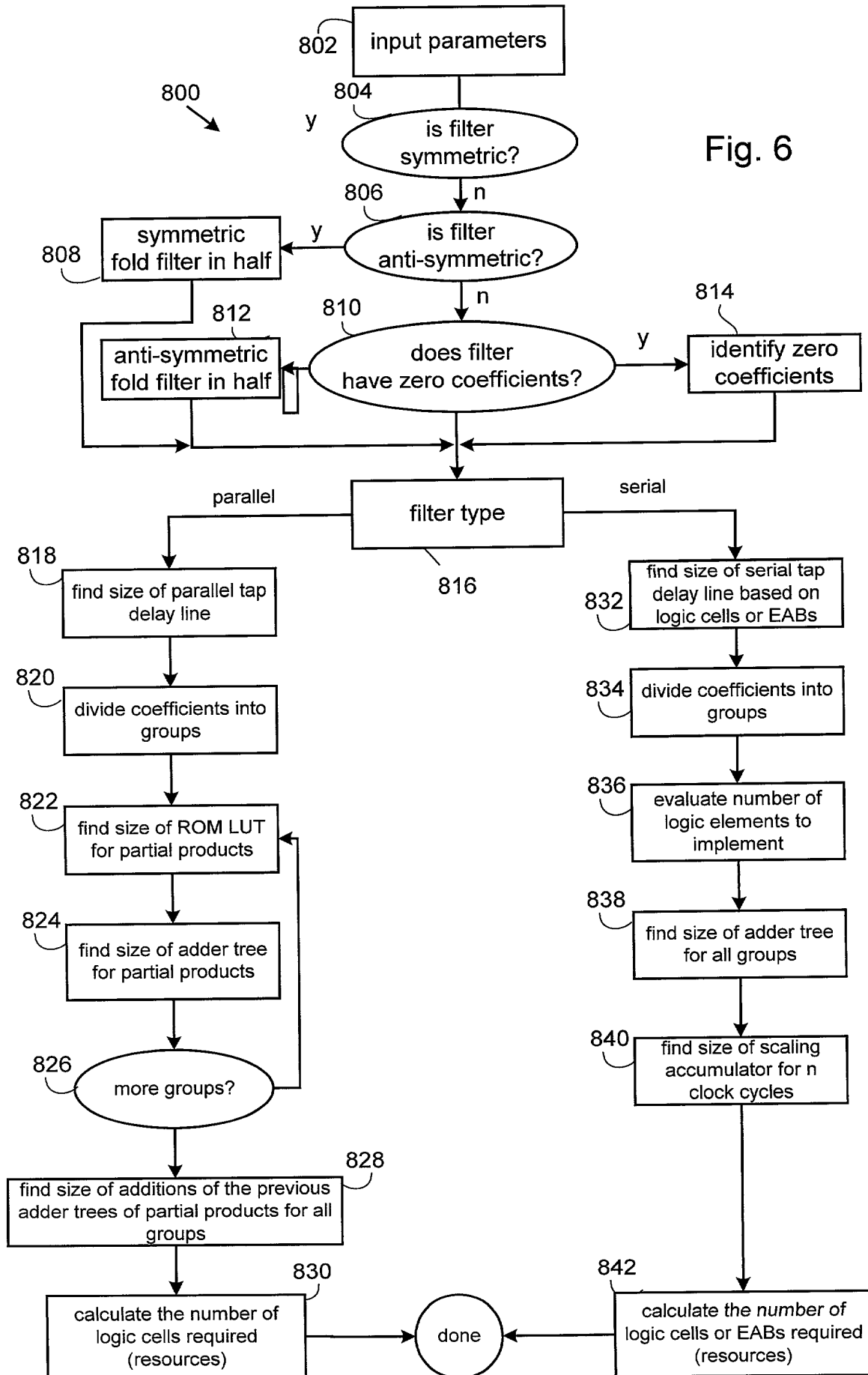


Fig. 4

Fig. 5





900

NUMBER OF INPUT BITS 902

SIGNED 904 UNSIGNED 906

CANCEL BACK APPLY NEXT

INPUT DATA BUS PARAMETERS

Fig. 7

1000

GENERATE
COEFFICIENT
VALUES 1006

READ COEFFICIENTS
FROM FILE 1004

ANALYZE FIXED
POINT
COEFFICIENTS

FLOATING POINT TO FIXED POINT CONVERSION

☐ NO CONVERSION

☐ SCALE TO USE UP TO

1008

 BITS OF PRECISION

☐ USE ONLY POWER OF TWO SCALING FACTORS

☐ SCALE BY FACTOR OF

SYMMETRY TYPE

1010

1002

COEFFICIENT VALUES

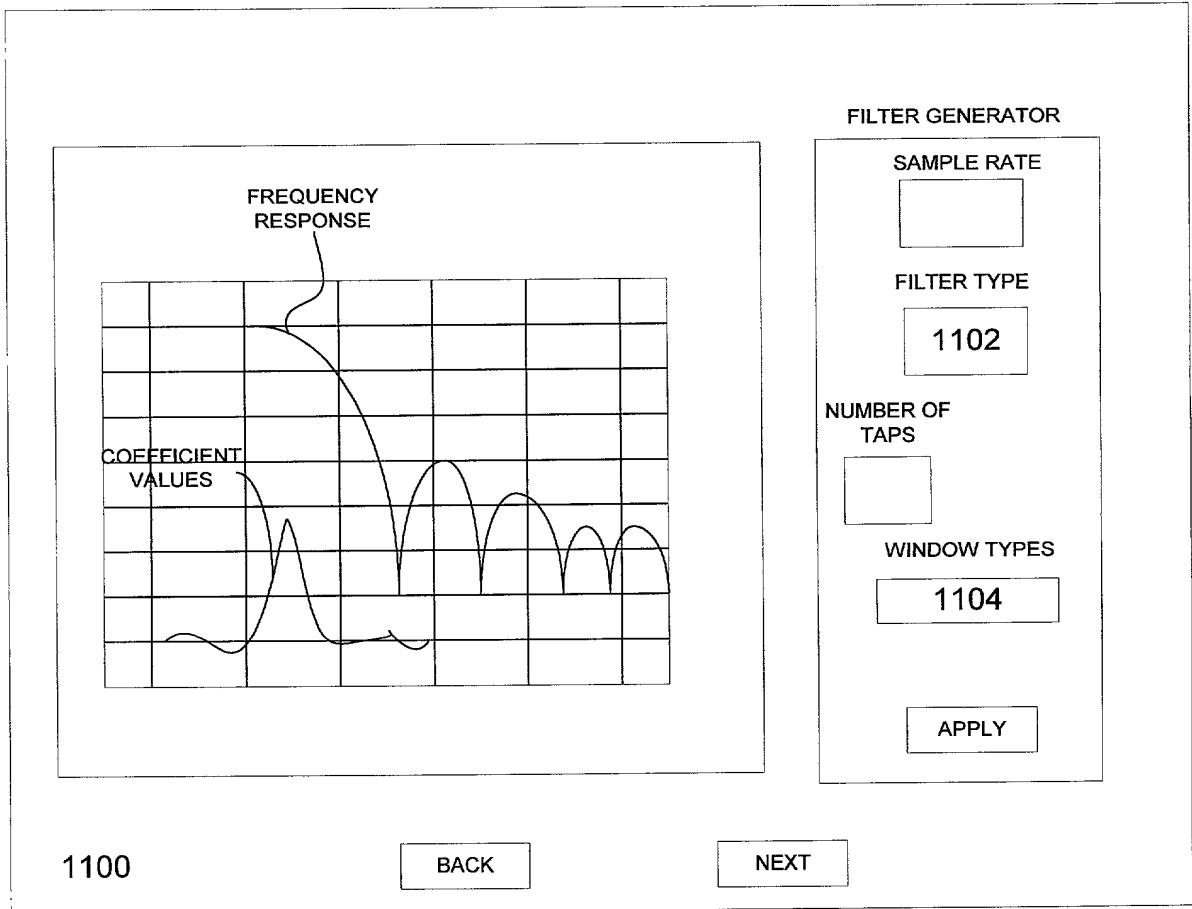
CANCEL

BACK

NEXT

SPECIFY COEFFICIENTS

Fig. 8



SCALED AND ROUNDED COEFFICIENTS

Fig. 9

GENERATE
COEFFICIENT
VALUES

READ
COEFFICIENTS
FROM FILE

ANALYZE FIXED
POINT
COEFFICIENTS

FLOATING POINT TO FIXED POINT CONVERSION

☐ NO CONVERSION

☐ SCALE TO USE UP TO BITS OF PRECISION

☐ USE ONLY POWER OF TWO SCALING FACTORS

☐ SCALE BY FACTOR OF

SYMMETRY TYPE

POSITIVE SYMMETRY

XXX.XX
XXX.XX
XXX.XX
XXX.XX

COEFFICIENT VALUES

CANCEL

BACK

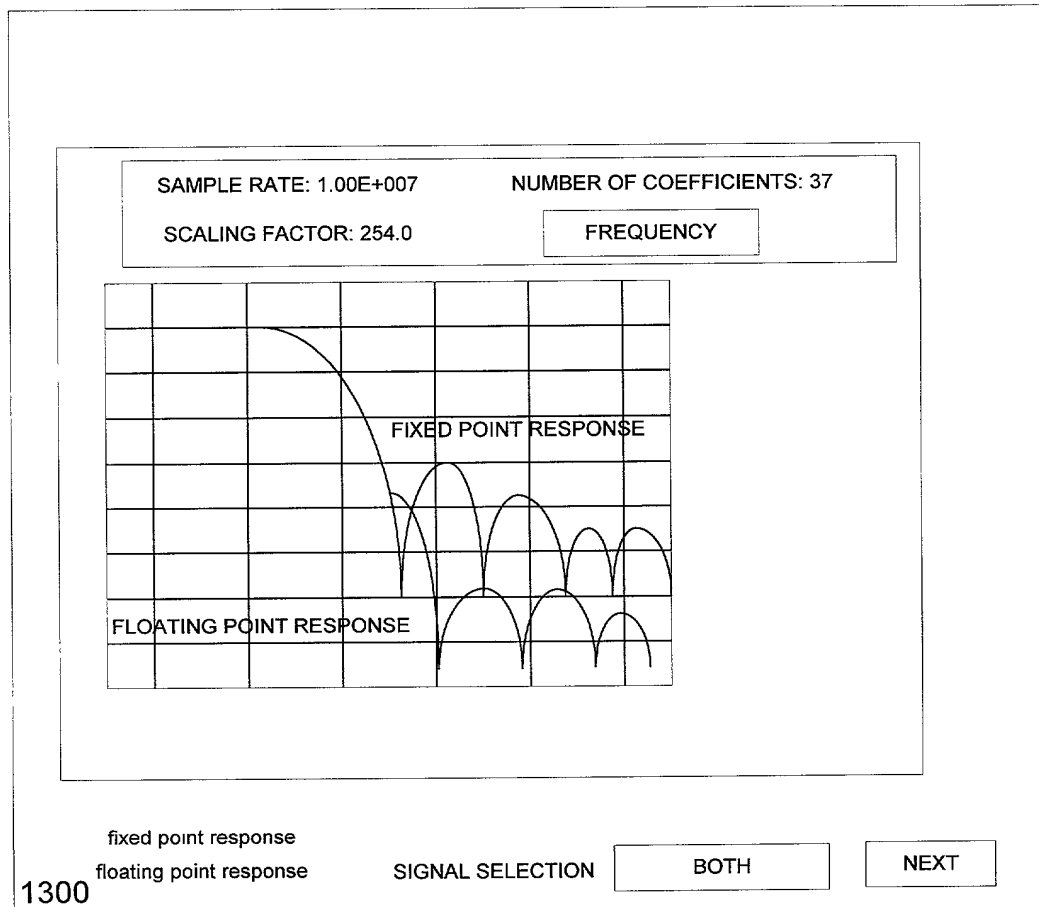
APPLY

NEXT

1200

SPECIFY COEFFICIENTS

Fig. 10



FIXED POINT COEFFICIENT ANALYZER

Fig. 11

1400

OUTPUT RESOLUTION (YOUT)

☐ FULL PRECISION ☒ LIMITED PRECISION

MSB

BITS REMOVED FROM MSB

☐ SATURATE ☒ TRUNCATE

LSB

BITS REMOVED FROM LSB

☐ ROUND ☒ TRUNCATE

SPECIFY FILTER PRECISION

Fig. 12

☐ DECIMATION
DECIMATION FACTOR

☐ INTERPOLATION
INTERPOLATION FACTOR

CANCEL

BACK

APPLY

NEXT

1500

SPECIFY DECIMATION OR INTERPOLATION

Fig. 13

ARCHITECTURE

NUMBER OF INPUT CHANNELS

PARALLEL IMPLEMENTATION ☐

SERIAL IMPLEMENTATION ☒

PIPELINING OPTIONS

SPEED OPTIMIZED ☐

AREA OPTIMIZED ☐

ESTIMATED RESOURCES OPTIONS

SIZE ESTIMATE 180 LOGIC CELLS 1602

3 DUAL PORT ESB/EAB

COMPUTATION TIME 4 CLOCK CYCLES PER INPUT

4 CLOCK CYCLES PER OUTPUT

CANCEL BACK APPLY NEXT

1600

SPECIFY FILTER ARCHITECTURE

Fig. 14

SIMULATION OUTPUT FILES

SIMULATION CLOCK PERIOD	FILE FORMAT
<div>40 NS</div>	<div><input type="checkbox"/> MAX+PLUS2 VECTOR FILE</div> <div><input type="checkbox"/> MATLAB SIMULINK MODEL</div> <div><input type="checkbox"/> MATLAB TESTBENCH MODEL</div> <div><input type="checkbox"/> VERILOG MODEL</div> <div><input checked="" type="checkbox"/> VHDL MODEL</div>

CHOOSE OUTPUT FILE TYPES

Fig. 15

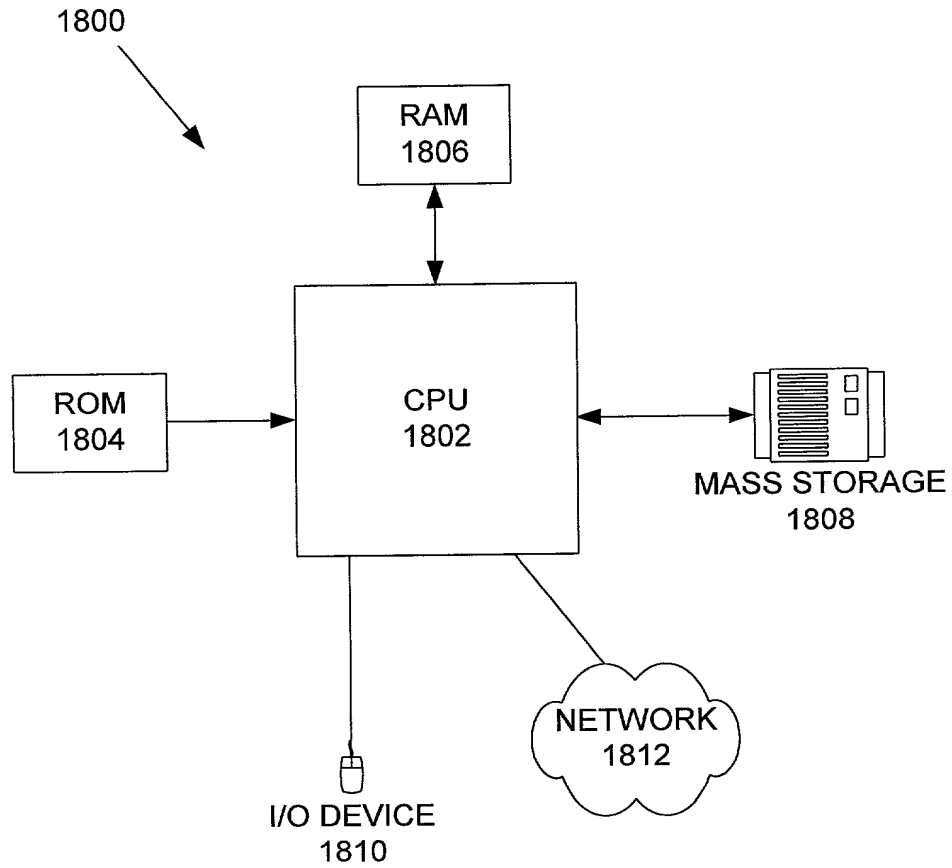


Fig. 16